WHAT IS CLAIMED IS:

1. A lead frame comprising:

a frame;

a ground ring disposed within the frame and defining:

a generally planar first ground ring surface;

a generally planar second ground ring surface disposed in opposed relation to the first ground ring surface; and

a plurality of third ground ring surfaces formed between the first and second ground ring surfaces in opposed relation to the first ground ring surface;

a chip mounting board disposed within the ground ring;

a plurality of tie bars connected to and extending between the frame, the ground ring and the chip mounting board for supporting the ground ring and the chip mounting board within the frame; and

a plurality of leads connected to the frame and extending about the periphery of the ground ring in spaced relation thereto.

2. The lead frame of Claim 1 wherein the chip mounting board defines:

a generally planar first board surface;

a generally planar second board surface disposed in opposed relation to the first board surface; and

a third board surface formed between the first and second board surfaces in opposed relation to the first board surface, the third board surface circumventing the second board surface.

3. The lead frame of Claim 2 wherein each of the tie bars defines:

a generally planar first tie bar surface;

a generally planar second tie bar surface disposed in opposed relation to the first tie bar surface; and

a third tie bar surface formed between the first and second tie bar surfaces in opposed relation to the first tie bar surface, the third tie bar surface being disposed between the frame and the ground ring.

4. The lead frame of Claim 2 wherein each of the leads defines:

a generally planar first lead surface;

a generally planar second lead surface disposed in opposed relation to the first lead surface; and

a third lead surface formed between the first and second lead surfaces in opposed relation to the first lead surface, the third lead surface being oriented closer to the ground ring than the second lead surface.

5. The lead frame of Claim 1 further comprising a plurality of slots formed between the ground ring and the chip mounting board.

6. The lead frame of Claim 1 further comprising a plurality of holes formed between the ground ring and the chip mounting board.

7. A semiconductor package comprising:

a lead frame comprising:

a frame;

a ground ring disposed within the frame and defining:

a generally planar first ground ring surface;

a generally planar second ground ring surface disposed in opposed relation to the first ground ring surface; and

a plurality of third ground ring

surfaces formed between the first and second ground ring surfaces in opposed relation to the first ground ring surface;

a chip mounting board disposed within the ground ring;

a plurality of tie bars connected to and extending between the frame, the ground ring and the chip mounting board for supporting the ground ring and the chip mounting board within the frame;

a plurality of leads connected to the frame and extending about the periphery of the ground ring in spaced relation thereto;

a semiconductor chip attached to the chip mounting board and including a plurality of input-output pads;

at least two conductive wires mechanically and electrically connecting respective ones of the input-output pads of the semiconductor chip to respective ones of the ground ring and the leads; and

a sealing part for sealing the chip mounting board, the ground ring, the tie bars, the leads, the semiconductor chip and the conductive wires, the sealing part being configured such that the second surface of the ground ring is exposed therewithin.

8. The semiconductor package of Claim 7 wherein the chip mounting board defines:

a generally planar first board surface;

a generally planar second board surface disposed in opposed relation to the first board surface; and

a third board surface formed between the first and second board surfaces in opposed relation to the first board surface, the third board surface circumventing the second board surface;

the semiconductor chip being attached to the first board surface of the chip mounting board.

9. The semiconductor package of Claim 8 wherein each of the tie bars defines:

a generally planar first tie bar surface;

a generally planar second tie bar surface disposed in opposed relation to the first tie bar surface; and

a third tie bar surface formed between the first and second tie bar surfaces in opposed relation to the first tie bar surface, the third tie bar surface being disposed between the frame and the ground ring.

10. The semiconductor package of Claim 9 wherein each of the leads defines:

a generally planar first lead surface;

a generally planar second lead surface disposed in opposed relation to the first lead surface; and

a third lead surface formed between the first and second third lead surfaces in opposed relation to the first lead surface, the third lead surface being oriented closer to the ground ring than the second lead surface.

11. The semiconductor package of Claim 10 wherein the sealing part is configured such that the second board surface of the chip mounting board, the second ground ring surface of the ground ring, the second tie bar surface of each of the tie bars, and the second lead surface of each of the leads are exposed therewithin.

12. The semiconductor package of Claim 8 wherein the semiconductor chip is attached to the first board surface via an adhesive layer.

13. The semiconductor package of Claim 7 wherein the conductive wire is connected to a portion of the first ground ring surface of the ground ring which is not disposed in opposed relation to any of the third ground ring surfaces.

14. A method of manufacturing a semiconductor

package, comprising the steps of:

a) preparing a lead frame which includes:

a frame;

a ground ring disposed within the frame and defining:

a generally planar first ground ring surface;

a generally planar second ground ring surface disposed in opposed relation to the first ground ring surface; and

a plurality of third ground ring surfaces formed between the first and second ground ring surfaces in opposed relation to the first ground ring surface;

a chip mounting board disposed within the ground ring;

a plurality of tie bars connected to and extending between the frame, the ground ring and the chip mounting board for supporting the ground ring and the chip mounting board within the frame; and

a plurality of leads connected to the frame and extending about the periphery of the ground ring in spaced relation thereto;

b) attaching a semiconductor chip having a plurality of input-output pads to the chip mounting board;

c) mechanically and electrically connecting the input-output pads of the semiconductor chip to respective ones of the leads and the first ground ring surface of the ground ring via at least two conductive wires;

d) partially encapsulating the chip mounting board, the ground ring, the tie bars, the leads, the semiconductor chip and the conductive wires with a

sealing part such that the second ground ring surface of the ground ring is exposed; and

e) cutting portions of the leads and the tie bars extending from the sealing part.

15. The method of Claim 14 wherein step (a) comprises preparing the lead frame such that the chip mounting board defines:

a generally planar first board surface;

a generally planar second board surface disposed in opposed relation to the first board surface; and

a generally planar third board surface formed between the first and second board surfaces in opposed relation to the first board surface and circumventing the second board surface.

16. The method of Claim 15 wherein step (a) further comprises preparing the lead frame such that each of the tie bars defines:

a generally planar first tie bar surface;

a generally planar second tie bar surface disposed in opposed relation to the first tie bar surface; and

a third tie bar surface formed between the first and second tie bar surfaces in opposed relation to the first tie bar surface, the third tie bar surface being disposed between the frame and the ground ring.

17. The method of Claim 16 wherein step (a) further comprises preparing the lead frame such that each of the leads defines:

a generally planar first lead surface;

a generally planar second lead surface disposed in opposed relation to the first lead surface; and

a third lead surface formed between the first and second third lead surfaces in opposed relation to the first lead surface, the third lead surface being oriented closer to the ground ring than the second

lead surface.

18. The method of Claim 17 wherein:

step (b) comprises attaching the semiconductor chip to the first board surface of the chip mounting board; and

step (d) comprises partially encapsulating the chip mounting board, the ground ring, the tie bars, the leads, the semiconductor chip and the conductive wires within the sealing part such that the second board surface of the chip mounting board, the second tie bar surface of each of the tie bars, the second ground ring surface of the ground ring, and the second lead surface of each of the leads are exposed.

19. The method of Claim 14 wherein step (b) comprises adhesively bonding the semiconductor chip to the chip mounting board.

20. The method of Claim 14 wherein step (e) comprises sawing the leads and the tie bars in a saw singulation process.

21. The method of Claim 14 wherein step (c) comprises bonding at least one of the conductive wires to a portion of the first ground ring surface disposed in opposed relation to the second ground ring surface.